A GAAS IC BROADBAND VARIABLE RING OSCILLATOR AND ARBITRARY INTEGER DIVIDER

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Abstract

A single GaAs IC performs as a broadband variable ring oscillator (VRO) and arbitrary integer frequency divider. The oscillator, a ring of inverters with a variable delay feature, covers two octaves in the 0.4 to 1.6 GHz range without external tuning elements, and is theoretically arbitrarily extendable lower in frequency. A provision for external signal injection enables injection locking. Frequency division is acheived with selectable arbitrary division ratio by tuning the oscillator to near the desired submultiple of the input signal. Spur-free output with constant amplitude is maintained independent of divide ratio.

Introduction

Modern broadband microwave oscillators are usually YIG or varactor tuned oscillators. YIG oscillators are very broadband and spectrally pure, but expensive, mechanically tedious, slow-tuning, and power-consumptive. Varactor oscillators are cheaper, faster tuning, and less power consumptive, but less broadband. In both cases active devices and resonating structures are in different physical media. In this paper we present a broadband variable ring oscillator (VRO), an integrated oscillator wherein feedback signal delay, and therefore oscillatory frequency, is continuously variable over more than two octaves[1,2]. The VRO is rapidly tunable and thus capable of broadband PM and FM. We believe the VRO establishes a new segment towards the lower end of the broadband oscillator cost/performance tradeoff continuum.

This VRO implementation also contains provision for injection-locking onto an arbitrary submultiple of an external signal. In this mode, it operates as a broadband frequency divider of arbitrary divide ratio. As opposed to other arbitrary divide ratio dividers such as counters and dual-modulus prescalars, the VRO-based divider maintains spurious-free and constant amplitude output, independent of divide ratio.

Oscillator

The intuitive explanation of the VRO concept is illustrated in Fig. 1. If the potentiometer's wiper arm is adjusted to the upper end, a high frequency three-stage ring oscillator results. If the potentiometer's wiper arm is at the lower end, a lower frequency five-stage oscillator results. If the wiper is set mid-range, the feedback signal is 50% three-stage-delay, plus 50% five-stage-delay, effectively equaling a four-stage-delay ring oscillator. If four inversion stages by themselves were hardwired in a ring, the circuit would not oscillate because the feedback signal would not reverse previous logic states. But in the present case proper (inverting) phase is maintained by tapping at the outputs of odd inverter stages. The circuit of Fig. 1 would provide a 5 to 3 tuning range.

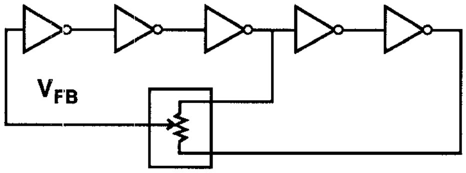

Figure 1. Intuitive variable ring oscillator (VRO) illustration.

In an actual circuit, the potentiometer is replaced with a Gilbert multiplier (which also provides an inversion), and frequency range is extended by adding more inverters and Gilbert multipliers. We present the results of the configuration shown in Fig. 2. In theory this would give a 13 to 3 (ratio of maximum to minimum inversion stages), or 4.33 to 1 tuning range. The circuit, fabricated in a 14 GHz f_t GaAs IC process [3], is shown in Fig. 3. Measured tuning range, shown in Fig. 4, was 0.376 to 1.58 GHz, or 4.20 to 1 (slightly more than two octaves). Note that the configuration can be further extended to lower frequencies by adding yet more inverters and Gilbert multipliers, or integrating static frequency dividers on-chip.

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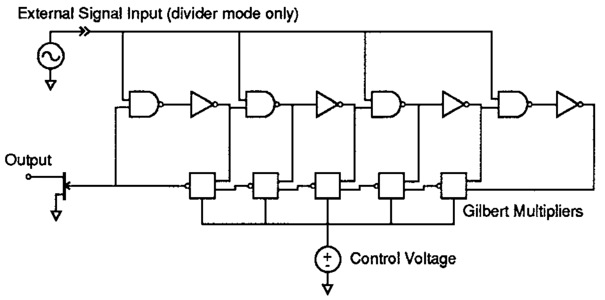

Figure 2. Two octave variable ring oscillator block diagram.

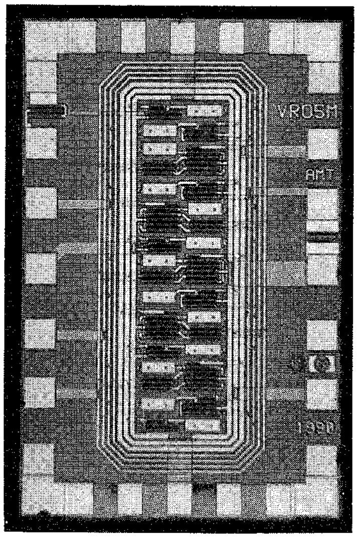

Figure 3. Variable ring oscillator circuit. The "racetrack" structure is power supply distribution, not a resonating structure.

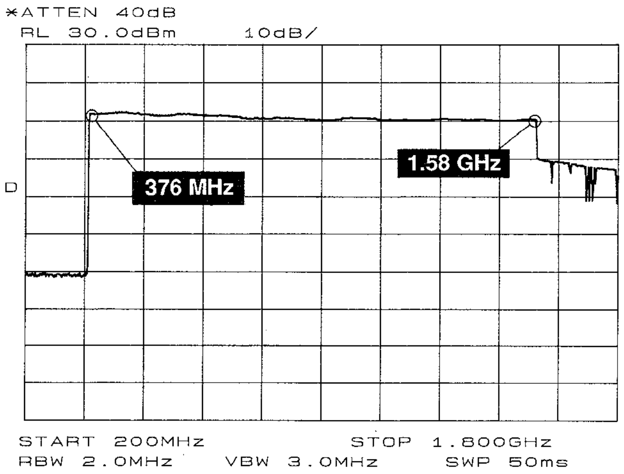

Figure 4. Oscillator runing range.

Oscillator stability at three frequencies measured on a HP8562A spectrum analyzer is shown in Fig. 5. The phase noise is high but this should not be a surprise given that the natural oscillatory frequency is controlled by low-Q logic gate delays. These delays are susceptable to the high 1/f noise of GaAs MESFETs, and one would expect improvement by migration of the circuit to a silicon BJT or GaAs HJBT process. In return for high phase noise, this oscillator has a fast tuning rate.

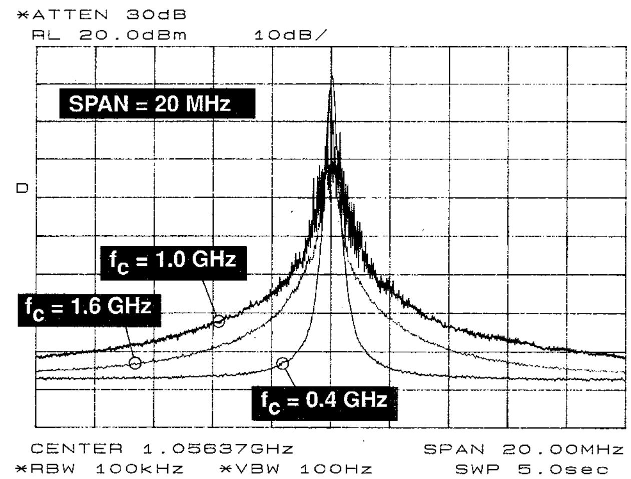

Figure 5. Oscillator stability at 0.4, 1.0, and 1.6 GHz (low end, midband, and high end).

Phase noise is best at lowest frequencies, poorer at highest frequencies, and worst midband. First we compare highest frequency versus lowest frequency phase noise. Adding an additional logic gate adds an incremental amount of delay, and an incremental amount of (uncorrelated) noise. As frequency is lowered by adding more logic gates, each added logic gate adds a linear amount of time delay but a sublinear amount of jitter (because the noise is uncorrelated). Thus, at lower frequencies, jitter becomes a smaller fraction of the total delay, and the ratio, i.e. phase noise, improves.

The very poor midband phase noise has topological origins. Given rise and fall times that are faster than delay times, voltage waveform "flat spots" will result. Consider, for example, the output at the potentiometer wiper arm in Fig. 2 when the wiper is centered. The wiper voltage waveform will first transition to 50% of its final value, flatten for about two propagation delays, then make a second transition to its final value. The flat spot in the waveform occurs at or near the logic threshold. Therefore the exact timing of the logic switch, in the presence of noise, is uncertain, and translates into phase noise. Remedies include increasing rise and fall times relative to delay times, and designing such that only one Gilbert multiplier and its nearest neighbors are active for any given control voltage setting.

f_t (GHz)	P_{in}(dBm)	$V_{control}$(V)	f_{out}(GHz)	P_{out}(dBm)	Divide ratio	Lock range at output (MHz)
1.400	+15	-0.41	1.400	+11.5	1	100
1.400	+15	+0.15	0.700	+12.7	2	17
1.400	+15	+0.42	0.467	+12.8	3	50
3.000	+15	-0.61	1.500	+10.7	4	110
3.000	+15	+0.22	0.600	+11.7	5	15
3.000	+15	+0.33	0.500	+12.7	6	3
3.000	+15	+0.67	1.000	+12.7	7	2
12.00	+15	-0.65	1.500	+11.0	8	9
12.00	+15	-0.41	1.333	+11.2	9	3
12.00	+15	-0.22	1.200	+11.0	10	5
12.00	+15	-0.14	1.091	+11.7	11	6
12.00	+15	-0.08	1.000	+10.8	12	2
12.00	+15	-0.02	0.923	+11.2	13	0.1
12.00	+15	+0.02	0.857	+11.3	14	2
12.00	+15	+0.06	0.800	+11.3	15	1

Table 1. Parameters of frequency division.

Frequency Divider

Several of the oscillator's inversion stages are NAND gates, into which an external signal may be injected. If the oscillator is tuned close to the external signal's frequency, or a submultiple thereof, the oscillator will injection lock. The lockup and frequency division process can be described as follows. Assume all signals are square waves and consider, for example, rising edges. Lockup occurs when the rising edge of the oscillator's signal arrives at the input of a NAND gate coincident with a rising edge of the injected signal. Lockup can occur if this coincidence occurs on *every* rising edge of the input injection signal, or *every other* rising edge, or *every third* rising edge, etc.

Injection-locked frequency division is not a new concept [4], but most implementations have are fixed either in divide ratio and/or output frequency [5,6]. The present implementation provides selectable divide ratio in an inherently broadband configuration, and maintains spur-free constant amplitude output for all divide ratios.

Some examples of frequency division are shown in Table 1. Arbitrary integer divide ratios are possible as long as the output frequency is within the natural tuning range of the oscillator. Lock range is narrow, varying from about 110 MHz (referred to the output) for higher output frequencies and low divide ratios, down to a very narrow 100 kHz at lower output frequencies and high divide ratios. Improving the lock range would greatly increase this circuit's usefulness. Input frequency range is quite wide, with divide-by-14 having been accomplished at an input frequency of 19.625 GHz. Lock range in this case however approached zero, and the circuit easily fell out of lock. Divide ratios of 2.5, 3.5, and 4.5 were also observed. In this case an internally generated harmonic of the input signal is being divided.

Conclusions

A monolithic broadband variable ring oscillator has been described. The oscillator tuning range is greater than two octaves without external tuning elements, and may be increased by extension of the basic topology. The oscillator can be injection-locked to a arbitrary submultiple of an input signal, resulting in frequency division by arbitrary division ratios. The present configuration is constrained by narrow frequency lock range, but maintains spur-free constant amplitude output independent of divide ratio.

Acknowledgements

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